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Total Number of Pages in This Submission	23

Application Number	10/730,713
Filing Date	26 NOV 2003
First Named Inventor	Sun et al.
Art Unit	2878
Examiner Name	Don Williams
Attorney Docket Number	79777

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☑ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
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Remarks

Response to Notice of Non-Compliant Appeal Brief (37 CFR 41.37)

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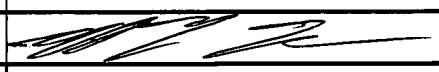
Signature			
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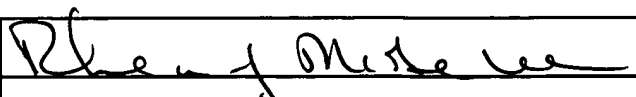
Signature			
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No:	**10/730,713**	Examiner:	**Tony W. Lu**
Filing Date:	**November 26, 2003**	Art Unit:	**2878**
Appellant:	**Sun et al.**	TC:	**2800**

Title: **METHOD AND APPARATUS FOR AN OPTICALLY CLOCKED OPTOELECTRONIC TRACK AND HOLD DEVICE**

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October 11, 2006

APPELLANT'S APPEAL BRIEF UNDER 37 C.F.R. §41

Sir:

In response to the Examiner's Office Action dated September 28, 2006, this is an amended appeal brief in response to the Final Office Action dated May 5, 2006. This is an appeal from the final rejection of Claims 1, 3, 5-12 and 15-20 and objection to Claims 13 and 14

by the Examiner. Claims 1, 3 and 5-20 are set forth in a Claims Appendix hereto, and together comprise all remaining Claims in the application. Appellant mailed a Notice of Appeal on July 27, 2006. Appellant received a return postcard indicating that the United States Patent and Trademark Office (PTO) received the Notice of Appeal on August 2, 2006.

REAL PARTY IN INTEREST

Under Title 15, section 3710c, an inventor who assigns his invention to the United States Government is entitled to at least 15 percent of any royalties that the Government receives upon licensing his invention. In this instance, two inventors, Chen-Kuo Sun and Donald J. Albares, qualify for this entitlement as they have assigned rights to this invention to the Government.

Chen-Kuo Sun and Donald J. Albares also qualify to receive incentive awards that take the form of "bonuses." These bonuses are due upon the Government inventor's case being authorized by Navy legal counsel for filing in the PTO and again when a Notice of Allowance is issued by the PTO. Additional financial awards may later be given based upon the value of the invention to the Navy.

The United States Government stands to gain financially from the present patent application. Besides receiving the defensive benefits of the patent, to which a largely subjective financial gain may be realized, the Government also stands to gain if the invention is licensed. As described above, Chen-Kuo Sun and Donald J. Albares are each entitled to at least 15 percent of licensing royalties up to $150,000 dollars per inventor per year. Amounts above this must be approved by the President. The remainder of licensing royalties goes back into U.S. Government coffers.

RELATED APPEALS AND INTERFERENCES

No related appeals and interferences are known to exist in the present case.

STATUS OF CLAIMS

Claims 1, 3, 5, 7-10, 15-18 and 20 have been finally rejected under 35 U.S.C. 102(b) as being anticipated by **Sun et al.**, USPN 5,239,181 (hereinafter referred to as "**S1**"). Claims 6 and 9 have been rejected under 35 U.S.C. 103(a) as being anticipated by **S1** in view of **Macdonald et al.**, USPN 4,727,349 (hereinafter referred to as "**S2**"). Claim 11 has been rejected under 35 U.S.C. 103(a) as being anticipated by **S1** in view of **Taddiken**, USPN 5,455,584 (hereinafter referred to as "**S3**"). The rejection of Claims 1, 3, 5-12 and 15-20 and objection to Claims 13 and 14 is on appeal.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action dated May 5, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

The optically clocked optoelectronic track and hold apparatus [*FIG. 2, Ref. No. 202*] comprises:

a diode bridge comprising a first node [*FIG. 2, Ref. No. 230*], a second node [*FIG. 2, Ref. No. 232*], a third node [*FIG. 2, Ref. No. 234*], a fourth node [*FIG. 2, Ref. No. 236*] and a plurality of diodes, wherein the plurality of diodes comprises:

a first diode [*FIG. 2, Ref. No. 250*] having a cathode operatively coupled to the first node [*FIG. 2, Ref. No. 230*] and an anode operatively coupled to the second node [*FIG. 2, Ref. No. 232*];

a second diode [*FIG. 2, Ref. No. 252*] having a cathode operatively coupled to the third node [*FIG. 2, Ref. No. 234*] and an anode operatively coupled to the first node [*FIG. 2, Ref. No. 230*];

a third diode [*FIG. 2, Ref. No. 258*] having a cathode operatively coupled to the fourth node [*FIG. 2, Ref. No. 236*] and an anode operatively coupled to the second node [*FIG. 2, Ref. No. 232*];

a fourth diode [*FIG. 2, Ref. No. 260*] having a cathode operatively coupled to the third node [*FIG. 2, Ref. No. 234*] and an anode operatively coupled to the fourth node [*FIG. 2, Ref. No. 236*];

an input node, operatively coupled to the first node [*FIG. 2, Ref. No. 230*] of the diode bridge, capable of receiving an analog input signal [*FIG. 2, Ref. No. 204*];

a first current source [*FIG. 2, Ref. No. 242*], operatively coupled to the second node [*FIG. 2, Ref. No. 232*] of the diode bridge and a second current source [*FIG. 2, Ref. No. 244*], operatively coupled to the third node [*FIG. 2, Ref. No. 234*] of the diode bridge, and wherein the first and second current sources [*FIG. 2, Ref. Nos. 242, 244*] are capable of forward biasing the diode bridge;

a first photodetector [*FIG. 2, Ref. No. 220*] having a cathode operatively coupled to the second node [*FIG. 2, Ref. No. 232*] and an anode operatively coupled to a negative potential node and a second photodetector [*FIG. 2, Ref. No. 222*] having an anode operatively coupled to the third node [*FIG. 2, Ref. No. 234*] and a cathode operatively coupled to a positive potential node, and wherein the first and second photodetectors [*FIG. 2, Ref. Nos. 220, 222*]are capable of receiving an optical input clocking signal [*FIG. 2, Ref. Nos. 208, 210*], and capable of reverse

biasing and forward biasing the diode bridge in response to the optical input clocking signal [*FIG. 2, Ref. Nos. 208, 210*];

a hold capacitor [*FIG. 2, Ref. No. 280*], operatively coupled to the fourth node [*FIG. 2, Ref. No. 236*], capable of tracking the analog input signal [*FIG. 2, Ref. No. 204*] when the diode bridge is forward biased, and capable of holding the analog input signal [*FIG. 2, Ref. No. 204*] when the diode bridge switches from forward biased to reverse biased. [*Specification: page 5, line 10 to page 8, line 2*].

The method for optically clocked optoelectronic tracking and holding [*FIG. 7, Ref. No. 700*], the method comprising the steps of:

a) receiving an analog input signal and an optical input clocking signal [*FIG. 7, Ref. No. 710*];

b) determining whether an optical pulse is received by at least two photodetectors from said optical input clocking signal [*FIG. 7, Ref. No. 720*];

c) maintaining a diode bridge in forward bias and returning to STEP (a) if said optical pulse is not received from said optical input clocking signal [*FIG. 7, Ref. No. 730*];

d) switching said diode bridge to reverse bias for a desired time and returning to STEP (a) if said optical pulse is received from said optical input clocking signal [*FIG. 7, Ref. No. 740-760*]. [*Specification: page 12, line 27 to page 14, line 4*].

The optically clocked optoelectronic track and hold apparatus [*FIG. 2, Ref. No. 202*], comprising:

a) means for receiving an analog input signal and an optical input clocking signal [*FIG. 7, Ref. No. 710*];

b) means for determining whether an optical pulse is received by at least two

photodetectors from said optical input clocking signal [*FIG. 7, Ref. No. 720*];

c) means for maintaining a diode bridge in forward bias and returning to STEP (a) if said optical pulse is not received from said optical input clocking signal [*FIG. 7, Ref. No. 730*];

d) means for switching said diode bridge to reverse bias for a desired time and returning to STEP (a) if said optical pulse is received from said optical input clocking signal [*FIG. 7, Ref. No. 740-760*] . [*Specification: page 12, line 27 to page 14, line 4*] [*Specification: page 5, line 10 to page 8, line 2*].

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Should the 35 U.S.C. §102(b) rejection of Claims 1, 3, 5, 7-10, 15-18 and 20 be withdrawn when the rejection is based on **S1**?

II. Should the 35 U.S.C. §103(a) rejection of Claims 6 and 19 be withdrawn when the rejection is based on **S1** in view of **S2**?

III. Should the 35 U.S.C. §103(a) rejection of Claim 11 be withdrawn when the rejection is based on **S1** in view of **S3**?

ARGUMENT

I. The 35 U.S.C. §102(b) rejection of Claims 1, 3, 5, 7-10, 15-18 and 20 based on S1 should be withdrawn because S1 fails to disclose, teach or suggest a current source operatively coupled to a diode bridge.

The United States Code provides that a person shall be entitled to a patent unless:

the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States. 35 U.S.C. §102(b)

Appellants respectfully contend that the Examiner's 35 U.S.C. §102(b) rejection is improper because the present invention as defined by independent Claims 1, 15 and 20 and dependent Claims 3, 5, 7-10 and 16-18 are patentably distinguishable over **S1**.

Independent claim 1 is directed to an optically clocked optoelectronic track and hold apparatus including a diode bridge, a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge.

In stark contrast, **S1** fails to disclose, teach or suggest the above-recited limitations specified by Claim 1. **S1** discloses a bridge type optoelectronic sample and hold circuit including photodiodes coupled to a diode bridge. Appellants contend that **S1** does not include a diode bridge, a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge. The Examiner suggests that "V+ or S_2" is a first current source and "V- or S_1" is a second current source of FIG. 2 of reference **S1**. Appellants respectfully contend that the Examiner has misconstrued FIG. 2 of reference **S1**. Specifically, the term "current source" commonly (if not always) refers to a device that provides constant current. The photodiodes S_2 and S_1 of FIG. 2 of reference **S1** do not provide constant current because they provide varying levels of current depending on illumination pulses from laser 21 of FIG. 2 of reference **S1**.

S1 cannot result in the present invention as recited in independent Claim 1 because **S1** fails to disclose or remotely suggest depositing a metal layer over said substrate to fill cavities

formed by said 3-D photoresist microstructure; and removing said 3-D photoresist microstructure to form a 3-D metal microstructure. Appellants believe Claims 1, 16 and 20 further particularly points out and distinctly Claims these limitations absent from cited references of record. As discussed above, independent Claims 1, 16 and 20 are patentably distinguishable over **S1** and, as such, Claims depending from independent Claims 1, 16 and 20 (e.g., Claims 3, 5, 7-10 and 16-18) are, *a fortiori*, also patentably distinguishable over **S1**. Accordingly, Appellants respectfully submit that the rejection of Claims 1, 3, 5, 7-10, 15-18 and 20 has been traversed, and that independent Claims 1, 16 and 20 and corresponding dependent Claims 3, 5, 7-10 and 16-18 should now be allowed.

II. The 35 U.S.C. §103(a) rejection of Claims 6 and 19 based on S1 in view of S2 should be withdrawn because S1 and S2 fail to disclose, teach or suggest a current source operatively coupled to a diode bridge.

The Examiner has not presented a valid prima facie case for the obviousness of any of Claims 6 and 19 in the Final Office Action mailed on May 5, 2006. The basic requirements of a *prima facie* case of obviousness are set forth in MPEP §2143, which states:

> *"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."*

MPEP §2142 further states, in part, "*The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness.*" The Examiner fails to state a proper *prima facie* case for obviousness in rejecting each of Claims 6 and 19 under 35 U.S.C. §103(a) as being unpatentable over **S1** in view of **S2**. To establish a *prima facie*

case of obviousness, the three basic criteria must be met. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991). In rejecting Claims 6 and 19 under 35 U.S.C. §103(a), the Examiner has not met at least the all claim limitations requirements recited in *In re Vaeck.*

All Claim Limitations: Even when combined, the references recited by the Examiner neither teach nor suggest **all** limitations of Appellants' claimed invention. These arguments are separately set forth below.

Accordingly, in rejecting Claims 6 and 19 under 35 U.S.C. §103(a), the Examiner has not met at least the all claim limitations requirement recited in *In re Vaeck* and therefore has not presented a proper *prima facie* case for obviousness in rejecting Claims 6 and 19 under 35 U.S.C. §103(a). Although Appellants are therefore not properly charged with the burden of rebutting Examiner's assertions of obviousness, the following discussion demonstrates that, even when combined, the recited references do not teach or suggest **all** limitations of Appellants' claims.

None of the cited prior art teaches or suggests an optically clocked optoelectronic track and hold apparatus including a diode bridge, a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge.

The cited references **S1** and **S2** neither teach nor suggest a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge.

As described above, **S1** discloses a bridge type optoelectronic sample and hold circuit including photodiodes coupled to a diode bridge. The cited reference **S1** neither teaches nor suggests a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge.

S2 discloses a depleted channel photoconductor. The cited reference **S2** neither teaches nor suggests a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge. In addition, MPEP §2143.03 states that if any independent claim is non-obvious under 35 U.S.C §103, then any claim depending therefrom is nonobvious. Therefore, dependent claims, which depend from Claims 1 and 15 (e.g., Claims 6 and 9), are patentable over the cited references for the above-stated reasons.

III. The 35 U.S.C. §103(a) rejection of Claim 11 based on S1 in view of S3 should be withdrawn because S1 and S3 fail to disclose, teach or suggest a current source operatively coupled to a diode bridge.

The Examiner has not presented a valid prima facie case for the obviousness of any of Claims 6 and 19 in the Final Office Action mailed on May 5, 2006. The basic requirements of a *prima facie* case of obviousness are set forth in MPEP §2143, which states:

> *"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."*

MPEP §2142 further states, in part, "*The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness.*" The Examiner fails to state a

proper *prima facie* case for obviousness in rejecting Claim 11 under 35 U.S.C. §103(a) as being unpatentable over **S1** in view of **S3**. To establish a *prima facie* case of obviousness, the three basic criteria must be met. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991). In rejecting Claim 11 under 35 U.S.C. §103(a), the Examiner has not met at least the all claim limitations requirements recited in *In re Vaeck.*

All Claim Limitations: Even when combined, the references recited by the Examiner neither teach nor suggest **all** limitations of Appellants' claimed invention. These arguments are separately set forth below.

Accordingly, in rejecting Claims 6 and 19 under 35 U.S.C. §103(a), the Examiner has not met at least the all claim limitations requirement recited in *In re Vaeck* and therefore has not presented a proper *prima facie* case for obviousness in rejecting Claims 6 and 19 under 35 U.S.C. §103(a). Although Appellants are therefore not properly charged with the burden of rebutting Examiner's assertions of obviousness, the following discussion demonstrates that, even when combined, the recited references do not teach or suggest **all** limitations of Appellants' claims.

None of the cited prior art teaches or suggests an optically clocked optoelectronic track and hold apparatus including a diode bridge, a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge.

The cited references **S1** and **S3** neither teach nor suggest a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge.

As described above, **S1** discloses a bridge type optoelectronic sample and hold circuit including photodiodes coupled to a diode bridge. The cited reference **S1** neither teaches nor suggests a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge.

S3 discloses a high frequency high resolution quantizer. The cited reference **S3** neither teaches nor suggests a first current source operatively coupled to the second node of the diode bridge and a second current source operatively coupled to the third node of the diode bridge. In addition, MPEP §2143.03 states that if any independent claim is non-obvious under 35 U.S.C §103, then any claim depending therefrom is nonobvious. Therefore, dependent claims, which depend from Claims 1 and 15 (e.g., Claims 6 and 9), are patentable over the cited references for the above-stated reasons.

CONCLUSION

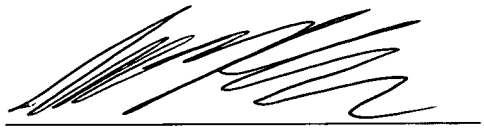
As discussed above, the pending claims of the current application are in condition for allowance because the Examiner has not presented a valid *prima facie* case for obviousness or lack of novelty. Appellants respectfully submit that all pending claims in this application are patentably distinguishable over any cited prior art references and not taught or disclosed by any cited prior art references. Accordingly, the rejection should be reversed and the Examiner directed to pass the case to issue.

The Commissioner is authorized to charge Deposit Account No. **50-0847** an amount of **$500.00** to pay the fee for filing a brief in support of an appeal per 37 C.F.R. §1.17(c). Please

charge any deficit or credit any excess to Deposit Account No. **50-0847**.

Respectfully submitted,

SPAWAR SYSTEMS CENTER SAN DIEGO
OFFICE OF PATENT COUNSEL 20012

By 

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CLAIMS APPENDIX

Claims Involved in the Appeal

CLAIM 1 (Previously Amended)

1. An optically clocked optoelectronic track and hold apparatus, comprising:

a) a diode bridge comprising a first node, a second node, a third node, a fourth node and a plurality of diodes, wherein said plurality of diodes comprises:

i) a first diode having a cathode operatively coupled to said first node and an anode operatively coupled to said second node;

ii) a second diode having a cathode operatively coupled to said third node and an anode operatively coupled to said first node;

iii) a third diode having a cathode operatively coupled to said fourth node and an anode operatively coupled to said second node;

iv) a fourth diode having a cathode operatively coupled to said third node and an anode operatively coupled to said fourth node;

b) an input node, operatively coupled to said first node of said diode bridge, capable of receiving an analog input signal;

c) a first current source, operatively coupled to said second node of said diode bridge and a second current source, operatively coupled to said third node of said diode bridge, and wherein said first and second current sources are capable of forward biasing said diode bridge;

d) a first photodetector having a cathode operatively coupled to said second node and an anode operatively coupled to a negative potential node and a second photodetector having an anode operatively coupled to said third node and a cathode operatively coupled to a positive potential node, and wherein said first and second photodetectors are capable of

receiving an optical input clocking signal, and capable of reverse biasing and forward biasing said diode bridge in response to said optical input clocking signal;

e) a hold capacitor, operatively coupled to said fourth node, capable of tracking said analog input signal when said diode bridge is forward biased, and capable of holding said analog input signal when said diode bridge switches from forward biased to reverse biased.

CLAIM 2 (Canceled)

2. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said current sources comprises a first current source and a second current source, and wherein said first current source is operatively coupled to said second node and said second current source is operatively coupled to said third node.

CLAIM 3 (Previously Amended)

3. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said first and second photodetectors are reverse biased by voltage sources.

CLAIM 4 (Canceled)

4. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said at least two photodetectors comprises a first photodiode and a second photodiode, and wherein said first photodiode is operatively coupled to said second node and said second photodiode is operatively coupled to said third node.

CLAIM 5 (Previously Amended)

5. The optically clocked optoelectronic track and hold apparatus of Claim 3, wherein said optical input clocking signal comprises a first optical input clocking signal and a second

optical input clocking signal, wherein said first photodetector is capable of receiving said first optical input clocking signal, and wherein said second photodetector is capable of receiving said second optical input clocking signal, and wherein said first optical input clocking signal and said second optical input clocking signal are synchronized.

CLAIM 6 (Previously Amended)

6. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said first and second photodetectors have fast rise times and long fall times.

CLAIM 7 (Previously Amended)

7. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said first and second photodetectors switch said diode bridge from forward biased to reverse biased when said optical input clocking signal illuminates said first and second photodetectors with an optical pulse.

CLAIM 8 (Previously Amended)

8. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said first and second photodetectors switches said diode bridge from reverse biased to forward biased when said first and second photodetectors do not generate enough photocurrent to reverse bias said diode bridge.

CLAIM 9 (Original)

9. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said optically clocked optoelectronic track and hold apparatus is configured into a positive node device and a negative node device, wherein said optically clocked optoelectronic track and

hold apparatus receives said analog input signal and an inverted analog input signal and outputs a differential output signal.

CLAIM 10 (Previously Amended)

10. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein said optically clocked optoelectronic track and hold apparatus further comprises an amplifier, operatively coupled to said hold capacitor, capable of outputting a first track and hold output signal.

CLAIM 11 (Previously Amended)

11. The optically clocked optoelectronic track and hold apparatus of Claim 10, wherein said optically clocked optoelectronic track and hold apparatus further comprises a quantizer, operatively coupled to said amplifier, capable of quantizing said first track and hold output signal and outputting a digital output signal.

CLAIM 12 (Previously Amended)

12. The optically clocked optoelectronic track and hold apparatus of Claim 10, wherein said optically clocked optoelectronic track and hold apparatus further comprises an electronic track and hold device, operatively coupled to said amplifier, capable of receiving said first track and hold output signal and an electronic clock signal, and wherein said electronic track and hold device is capable of outputting a second track and hold output signal.

CLAIM 13 (Previously Amended)

13. The optically clocked optoelectronic track and hold apparatus of Claim 1, wherein a photodetector of said first and second photodetectors comprises a short transit time photodiode and a long transit time photodiode in a parallel configuration.

CLAIM 14 (Original)

14. The optically clocked optoelectronic track and hold apparatus of Claim 13, wherein said short transit time photodiode and said long transit time photodiode are focus illuminated in I regions near junctions between P regions and N regions.

CLAIM 15 (Original)

15. A method for optically clocked optoelectronic tracking and holding, the method comprising the steps of:

a) receiving an analog input signal and an optical input clocking signal;

b) determining whether an optical pulse is received by at least two photodetectors from said optical input clocking signal;

c) maintaining a diode bridge in forward bias and returning to STEP (a) if said optical pulse is not received from said optical input clocking signal;

d) switching said diode bridge to reverse bias for a desired time and returning to STEP (a) if said optical pulse is received from said optical input clocking signal.

CLAIM 16 (Original)

16. The method of Claim 15, wherein said switching said diode bridge to reverse bias for a desired time step comprises the following sub-steps:

i) generating photocurrent sufficient to reverse bias said diode bridge if said optical pulse is received from said optical input clocking signal;

ii) maintaining sufficient photocurrent to reverse bias said diode bridge for said desired time;

iii) switching said diode bridge to forward bias when photocurrent becomes insufficient to reverse bias said diode bridge;

iv) returning to STEP (a) of Claim 15.

CLAIM 17 (Original)

17. The method of Claim 15, wherein said maintaining diode bridge in forward bias step comprises forward biasing said diode bridge by said at least two photodetectors not generating enough photocurrent.

CLAIM 18 (Original)

18. The method of Claim 15, wherein said switching said diode bridge to reverse bias for said desired time step comprises reverse biasing said diode bridge by said at least two photodetectors quickly switching to an on-state.

CLAIM 19 (Original)

19. The method of Claim 15, wherein said switching said diode bridge to reverse bias for said desired time step uses a long transit time photodiode to maintain sufficient photocurrent for said desired time.

CLAIM 20 (Original)

20. An optically clocked optoelectronic track and hold apparatus, comprising:

a) means for receiving an analog input signal and an optical input clocking signal;

b) means for determining whether an optical pulse is received by at least two photodetectors

from said optical input clocking signal;

c) means for maintaining a diode bridge in forward bias if said optical pulse is not received from said optical input clocking signal;

d) means for switching said diode bridge to reverse bias for a desired time if said optical pulse is received from said optical input clocking signal.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.